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FIshii001(10/698,620)

## PATENT

### IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

5 In re application of: Fusao Ishii : Date: September 12, 2008  
Serial No.: 10/698,620 : Group No.: 2873  
Filed: November 1, 2003 : Examiner: Brandi N. Thomas  
Attorney Docket No.: FIshii001 : @ (571) 272-2341 (T) 872-9306 (F)

#### CERTIFICATION UNDER 37 CFR 1.10

10 I hereby certify that this Office Response Transmittal and the documents referred to as enclosed therein are being deposited with the United States Postal Service on this date **September 12, 2008** in an envelope as "Express Mail Post Office to Addressee" Mailing Label Number **EB887275246 US** addressed to the: Commissioner of Patents and Trademarks, Alexandria, VA. 22313-1450.

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NOTE: Each paper or fee referred to as enclosed herein has the number of the "Express Mail" mailing label placed thereon to mailing. 37 CFR 1.10(b).

To the Commissioner of Patents and Trademarks:

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### AMENDMENT

Dear Sir:

30 In response to the Examiner's Action mailed on May 12, 2008, the Applicant hereby respectfully requests a one months extension with an extension fee of \$60 enclosed. Please amend the above referenced Patent Application be amended as set forth below.

35

I) Please amend claims 1 to 60 as set forth below:

September 12, 2008

1. (Currently Amended) An electromechanical micromirror device,  
comprising:

5 a single semiconductor substrate with a bottom surface and a top  
surface opposite said bottom surface;

a control circuitry disposed on said bottom surface of said single  
substrate; and

10 a micromirror section disposed on said top surface of said single  
semiconductor substrate;

wherein said micromirror section comprises  
a micromirror; and

15 at least one support structure for supporting said micromirror and  
via connectors opened through said single semiconductor substrate  
for connecting said control circuit to said support structure.

20 2. (Currently Amended ) 2. The device of claim 1, wherein:

said control circuitry disposed on said bottom surface of said single  
semiconductor substrate comprising a circuit selected from the  
group consisting of: CMOS circuits, NMOS circuits, PMOS circuits,  
25 bipolar circuits, BiCMOS circuits, DMOS circuits, HEMT circuits,  
amorphous silicon thin film transistor circuits, polysilicon thin film  
transistor circuits, SiGe transistor circuits, SiC transistor circuits,  
GaN transistor circuits, GaAs transistor circuits, InP transistor  
circuits, CdSe transistor circuits, organic transistor circuits, and  
30 conjugated polymer transistor circuits.